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CCM Operation Analysis of the Single-Phase Three-Level Quasi-Z-Source Inverter

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Abstract – This paper presents a CCM analysis of a new modification of a three-level single phase neutral-point-clamped inverter. The proposed topology combines advantages of the three-level neutral-point-clamped full-bridge inverter with those of the quasi-Z-source inverter. The three-level neutral-point-clamped quasi-Z-source inverter is especially suitable for renewable energy sources. The steady-state analysis of a three-level neutral-point-clamped quasi-Z-source inverter in the case of the continuous conduction mode is presented. The conditions of the continuous conduction mode are obtained and analyzed.

Keywords – Three-level neutral-point-clamped inverter, continuous conduction mode, quasi-Z-source inverter.

I. INTRODUCTION

A three-level neutral-point-clamped (3L-NPC) inverter (Fig. 1a) has a number of advantages over the two-level voltage source inverter, such as lower semiconductor voltage stress, lower required blocking voltage capability, decreased dv/dt , better harmonic performance, soft switching possibilities without additional components, higher switching frequency due to lower switching losses, and balanced neutral-point voltage. As a drawback, in contrast to the two-level voltage source inverter, it has two additional clamping diodes per phase-leg and more controlled semiconductor switches per phase-leg. The 3L-NPC can normally perform only the voltage buck operation. In order to ensure voltage boost operation an additional DC/DC boost converter should be used in the input stage [1-2].

To obtain buck and boost performance the focus is on a quasi-Z-source inverter (qZSI, Fig. 1b). The qZSI was first introduced in [3]. The qZSI can boost the input voltage by introducing a special shoot-through switching state, which is the simultaneous conduction (cross conduction) of both

switches of the same phase leg of the inverter [3-11]. This switching state is forbidden for traditional voltage source inverters because it causes a short circuit of the DC-link capacitors. Thus, the qZSI has excellent immunity against the cross conduction of the top and bottom-side inverter switches. The possibility of using shoot-through eliminates the need for dead-times without having the risk of damaging the inverter circuit.

Recently, a new modification of the qZSI was proposed: a three-level neutral point clamped quasi-Z-source inverter (3L-NPC qZSI). This topology combines advantages of the three-level neutral-point-clamped full-bridge inverter with those of the quasi-Z-source inverter having the buck-boost capability of the input voltage and the enhanced output voltage quality [12, 13].

Thanks to its specific properties the 3L-NPC qZSI is especially suitable as power conditioner for the renewable energy systems, where the continuous conduction mode operation (CCM) is a very important issue. During the CCM the input current never drops to zero, thus featuring the reduced stress of the input voltage source, which is especially topical in such demanding applications as power conditioners for fuel cells and solar panels. The opposite case, the discontinuous conduction mode (DCM) in the converter evokes additional losses in the system and increases the operating range of the components. It is particularly relevant in single phase inverters where consumption of instantaneous power is variable, leading to variable input current. As a result, the CCM condition is not easily achievable and has not been observed in similar converter topologies [6, 7].

This paper presents the steady-state analysis of a single phase 3L-NPC qZSI in the case of the CCM and discusses some design guidelines in order to maintain the CCM operation.

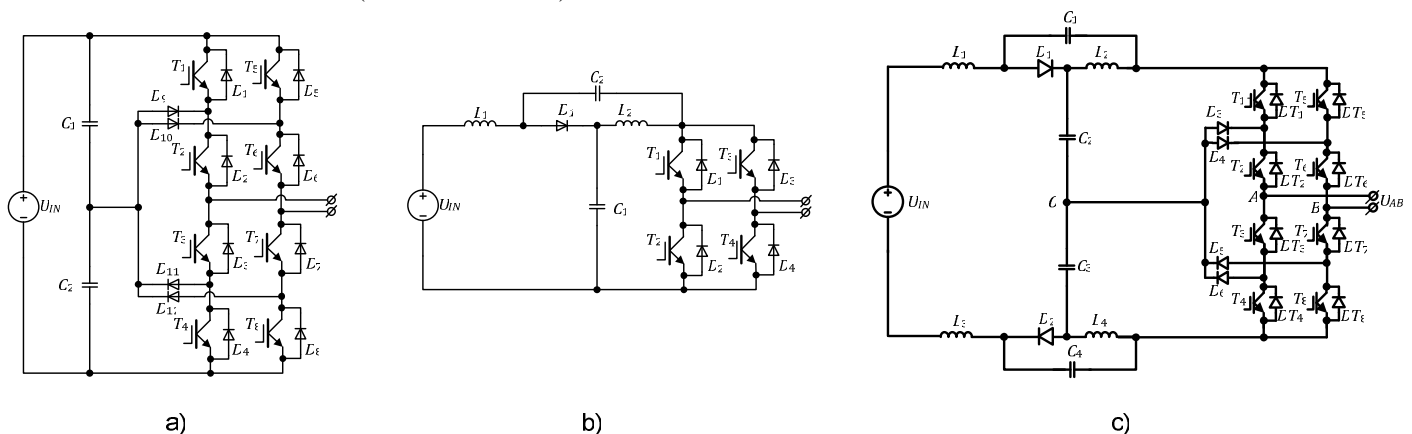


Fig. 1. Topologies of the 3L-NPC (a), qZSI (b) and 3L-NPC qZSI.

II. GENERAL DESCRIPTION AND STEADY-STATE ANALYSIS OF 3L-NPC QZSI

Fig. 1c illustrates the proposed topology of a 3L-NPC qZSI. Each leg of the 3L-NPC qZSI consists of two complementary switching pairs and four anti-parallel diodes. Advantages of this topology over the traditional two-level voltage source inverter are: continuous input current, use of shoot-through, lower switching losses, and balanced neutral-point voltage.

Shoot-through states are equally distributed over the operating period of the inverter. The inverter output voltage has three different levels: 0, $B \cdot (U_{IN}/2)$ and $B \cdot U_{IN}$ in the positive and negative directions, where B is the inverter boost factor. The shoot-through vector is generated separately. Finally, the shoot-through vector is mixed with other control signals.

In general, the operating period of the 3L-NPC qZSI in the continuous conduction mode (CCM) may be divided into 8 time intervals, as shown in Fig. 2. Transistor states for each time interval are depicted in Fig. 3. As it can be seen, all the switching states can be separated into three main modes: zero state (Fig 3a), active states (Fig 3c-h) and shoot-through state (Fig 3b). On the other hand, active states are separated on the three submodes.

An equivalent scheme for zero-state intervals is shown in Fig. 3a. Equations that describe the behavior of the converter in this mode are as follows:

$$U_{IN} - L_1 \frac{dI_{L1}}{dt} - U_{C2} - U_{C3} - L_3 \frac{dI_{L3}}{dt} = 0, \quad (1)$$

$$U_{C1} + L_2 \frac{dI_{L2}}{dt} = 0, \quad (2)$$

$$L_4 \frac{dI_{L4}}{dt} + U_{C4} = 0, \quad (3)$$

$$-I_{ZL} Z_L = 0, \quad (4)$$

$$I_{L1} = I_{L3}, \quad (5)$$

$$I_{L1} + C_1 \frac{dU_{C1}}{dt} - I_{L2} - C_2 \frac{dU_{C2}}{dt} = 0, \quad (6)$$

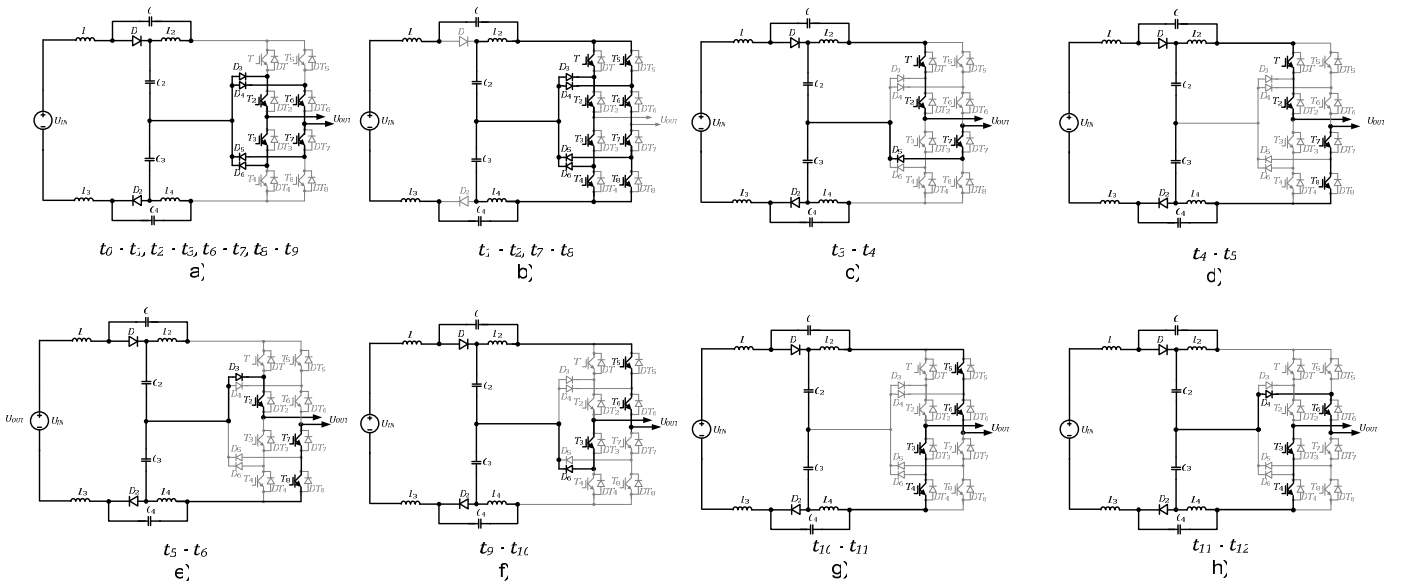


Fig. 2. Transistor states for each time interval.

$$C_3 \frac{dU_{C3}}{dt} + I_{L4} - C_4 \frac{dU_{C4}}{dt} - I_{L3} = 0, \quad (7)$$

$$C_2 \frac{dU_{C2}}{dt} - C_3 \frac{dU_{C3}}{dt} = 0, \quad (8)$$

$$U_{OUT} = I_{ZL} Z_L. \quad (9)$$

An equivalent scheme for the shoot-through intervals is shown in Fig. 3b. Equations that describe the behavior in this mode are as follows:

$$U_{IN} - L_1 \frac{dI_{L1}}{dt} + U_{C1} + U_{C4} - L_3 \frac{dI_{L3}}{dt} = 0, \quad (10)$$

$$U_{C2} - L_2 \frac{dI_{L2}}{dt} = 0, \quad (11)$$

$$U_{C3} - L_4 \frac{dI_{L4}}{dt} = 0, \quad (12)$$

$$I_{L1} = I_{L3}, \quad (13)$$

$$I_{L1} + C_1 \frac{dU_{C1}}{dt} = 0, \quad (14)$$

$$C_3 \frac{dU_{C3}}{dt} + I_{L4} = 0. \quad (15)$$

The first equivalent scheme for the active state is shown in Fig. 3c. It corresponds to the case when the output voltage is equal to half of the DC-link voltage. The middle point is clamped through the load to the high side of the DC-link. Equations (16) to (25) describe the behavior in this mode:

$$U_{IN} - L_1 \frac{dI_{L1}}{dt} - U_{C2} - U_{C3} - L_3 \frac{dI_{L3}}{dt} = 0, \quad (16)$$

$$U_{C1} + L_2 \frac{dI_{L2}}{dt} = 0, \quad (17)$$

$$L_4 \frac{dI_{L4}}{dt} + U_{C4} = 0, \quad (18)$$

$$U_{C2} - L_2 \frac{dI_{L2}}{dt} - U_{OUT} = 0, \quad (19)$$

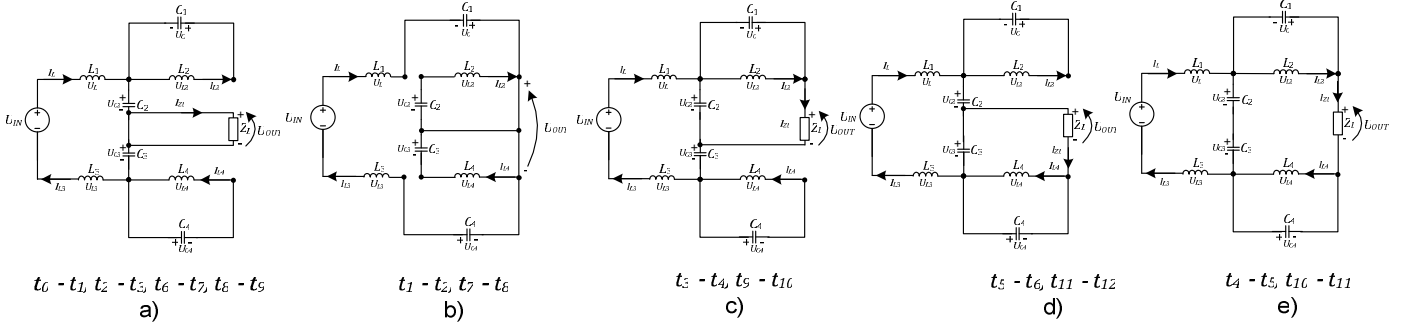


Fig. 3. Equivalent schemes of main operating modes.

$$I_{L1} = I_{L3}, \quad (20)$$

$$I_{L1} + C_1 \frac{dU_{C1}}{dt} - I_{L2} - C_2 \frac{dU_{C2}}{dt} = 0, \quad (21)$$

$$I_{L2} - C_1 \frac{dU_{C1}}{dt} - I_{ZL} = 0, \quad (22)$$

$$C_3 \frac{dU_{C3}}{dt} + I_{L4} - C_4 \frac{dU_{C4}}{dt} - I_{L3} = 0, \quad (23)$$

$$C_2 \frac{dU_{C2}}{dt} - C_3 \frac{dU_{C3}}{dt} + I_{ZL} = 0, \quad (24)$$

$$U_{OUT} = I_{ZL} Z_L. \quad (25)$$

The second equivalent scheme for the active state is shown in Fig. 3d. It corresponds to the case when the output voltage is equal to half of the DC-link voltage and the middle point is clamped through the load to the low side of the DC-link. Equations (26) to (35) describe the behavior in this mode:

$$U_{IN} - L_1 \frac{dI_{L1}}{dt} - U_{C2} - U_{C3} - L_3 \frac{dI_{L3}}{dt} = 0, \quad (26)$$

$$U_{C1} + L_2 \frac{dI_{L2}}{dt} = 0, \quad (27)$$

$$L_4 \frac{dI_{L4}}{dt} + U_{C4} = 0, \quad (28)$$

$$U_{C3} - U_{OUT} - L_4 \frac{dI_{L4}}{dt} = 0, \quad (29)$$

$$I_{L1} = I_{L3}, \quad (30)$$

$$I_{L1} + C_1 \frac{dU_{C1}}{dt} - I_{L2} - C_2 \frac{dU_{C2}}{dt} = 0, \quad (31)$$

$$I_{ZL} - I_{L4} + C_4 \frac{dU_{C4}}{dt} = 0, \quad (32)$$

$$C_3 \frac{dU_{C3}}{dt} + I_{L4} - C_4 \frac{dU_{C4}}{dt} - I_{L3} = 0, \quad (33)$$

$$C_2 \frac{dU_{C2}}{dt} - C_3 \frac{dU_{C3}}{dt} - I_{ZL} = 0, \quad (34)$$

$$U_{OUT} = I_{ZL} Z_L. \quad (35)$$

The third equivalent scheme for the active state is shown in Fig. 3e. It corresponds to the case when the output voltage is equal to the DC-link voltage. Equations (36) to (45) describe the behavior of the converter in this mode:

$$U_{IN} - L_1 \frac{dI_{L1}}{dt} - U_{C2} - U_{C3} - L_3 \frac{dI_{L3}}{dt} = 0, \quad (36)$$

$$U_{C1} + L_2 \frac{dI_{L2}}{dt} = 0, \quad (37)$$

$$L_4 \frac{dI_{L4}}{dt} + U_{C4} = 0, \quad (38)$$

$$U_{C3} + U_{C2} - L_2 \frac{dI_{L2}}{dt} - U_{OUT} - L_4 \frac{dI_{L4}}{dt} = 0, \quad (39)$$

$$I_{L1} = I_{L3}, \quad (40)$$

$$I_{L1} + C_1 \frac{dU_{C1}}{dt} - I_{L2} - C_2 \frac{dU_{C2}}{dt} = 0, \quad (41)$$

$$I_{ZL} - I_{L4} + C_4 \frac{dU_{C4}}{dt} = 0, \quad (42)$$

$$C_3 \frac{dU_{C3}}{dt} + I_{L4} - C_4 \frac{dU_{C4}}{dt} - I_{L3} = 0, \quad (43)$$

$$I_{L2} - C_1 \frac{dU_{C1}}{dt} - I_{ZL} = 0, \quad (44)$$

$$U_{OUT} = I_{ZL} Z_L. \quad (45)$$

To simplify the analysis it was assumed that the input capacitors and inductors are identical, thus:

$$L_1 = L_3, \quad L_2 = L_4, \quad (46)$$

$$C_1 = C_4, \quad C_2 = C_3. \quad (47)$$

The operating period of the converter in the CCM could be represented as

$$\frac{t_N}{T} + \frac{t_S}{T} = D_N + D_S = 1. \quad (48)$$

where D_N is the duty cycle of the non-shoot-through and D_S is the shoot-through duty cycle.

In the steady state the average voltage of the inductor over one switching period is zero and the voltages across the capacitors are constant. Thus, by Eqs. (1) to (45), the voltages across the capacitors can be found:

$$U_{C1} = U_{C4} = \frac{D_S \cdot U_{IN}}{2 - 4 \cdot D_S}, \quad (49)$$

$$U_{C2} = U_{C3} = \frac{U_{IN} \cdot (D_S - 1)}{4 \cdot D_S - 2}. \quad (50)$$

The peak DC-link voltage is the sum of all the capacitor voltages:

$$U_{DC} = U_{C1} + U_{C2} + U_{C3} + U_{C4} = \frac{U_{IN}}{1 - 2 \cdot D_S}. \quad (51)$$

Taking into account the maximum possible value of the modulation index $M=1-D_S$, the boost factor of the 3L-NPC

qZSI can be estimated as

$$B = \frac{U_{OUT_MAX}}{U_{IN}} = \frac{U_{DC} \cdot (1 - D_S)}{U_{IN}} = \frac{1 - D_S}{1 - 2 \cdot D_S}, \quad (52)$$

where U_{OUT_MAX} is an amplitude value of the output voltage.

III. CCM CONDITION AND SOME DESIGN GUIDELINES FOR THE 3L-NPC qZSI

In an ideal case, the DC-link voltage and the input current of the 3L-NPC qZSI are constant. The main problem lies in the floating instantaneous consuming power that evokes current fluctuations in the corresponding capacitors. A simplified equivalent scheme of the qZS network is shown in Fig. 4a. The capacitors and inductors are represented as ideal voltage and current sources, correspondingly. The idealized operating waveforms of the 3L-NPC qZSI are shown in Fig. 4b.

In a real system the operating waveforms are distorted by the ripple as shown in Fig. 4c. As it can be seen, the DC-link voltage has low frequency fluctuation (100 Hz) caused by instantaneous output power. As a result, it causes low frequency input current fluctuations. Also, it should be noticed that the input current has high frequency ripple. It is connected with the high frequency shoot-through duty cycle switching.

In order to eliminate low frequency fluctuations in the system it is necessary to maintain constant voltages across the capacitors despite the AC component present in the DC-link current.

Capacitor voltage ripple can be expressed as

$$\begin{aligned} \Delta U_{C1} = \Delta U_{C4} &= \frac{1}{C_1} \int_0^{T/4} i_C(t) dt = \\ &= \frac{1}{C_1} \int_0^{T/4} \frac{P_{OUT}}{U_{DC}} \cdot \sin\left(2 \cdot \frac{2\pi}{T} \cdot t\right) dt = \frac{T \cdot P_{OUT}}{2\pi \cdot C_1 \cdot U_{DC}}, \end{aligned} \quad (53)$$

where T is the period of the sinusoidal output voltage.

The required value of the capacitance of C_1 to maintain the desired voltage ripple factor K_C can be obtained using Eqs. (49), (52) and (53):

$$K_C = \frac{\Delta U_{C1}}{U_{C1}} = \frac{T \cdot P_{OUT} \cdot (1 - D_S)^2}{2\pi \cdot C_1 \cdot U_{OUT_MAX}^2 \cdot D_S}, \quad (54)$$

where K_C is the voltage ripple factor.

As a result, the capacitor can be calculated:

$$C_1 \geq \frac{T \cdot P_{OUT} \cdot (1 - D_S)^2}{2\pi \cdot K_C \cdot U_{OUT_MAX}^2 \cdot D_S}. \quad (55)$$

Capacitance values for capacitors C_2 , C_3 could be defined similarly:

$$C_2 \geq \frac{T \cdot P_{OUT} \cdot (1 - D_S)}{2\pi \cdot K_C \cdot U_{OUT_MAX}^2}. \quad (56)$$

A decrease in speed is defined by the equivalent schemes and it depends on the load resistance R . The rising speed depends on the inductor and capacitor voltages. It means that high frequency ripple of the current can be found from the shoot-through interval.

From Eq. (10) we obtain:

$$\begin{aligned} \Delta I_{L1} &= \int_0^{T_S \cdot D_S} \frac{dI_{L1}}{dt} \cdot dt = \int_0^{T_S \cdot D_S} \left(\frac{U_{IN} + U_{C1} + U_{C4}}{2 \cdot L} \right) \cdot dt = \\ &= \left(\frac{U_{IN} + U_{C1} + U_{C4}}{2 \cdot L} \right) \cdot T_S \cdot D_S, \end{aligned} \quad (57)$$

where T_S is the switching period. In order to maintain the CCM operation of the converter the input current ripple ΔI_{L1} should be smaller than the average input current I_a . The average input current can be defined from the power balance:

$$P_{IN} = U_{IN} \cdot I_a = P_{OUT}. \quad (58)$$

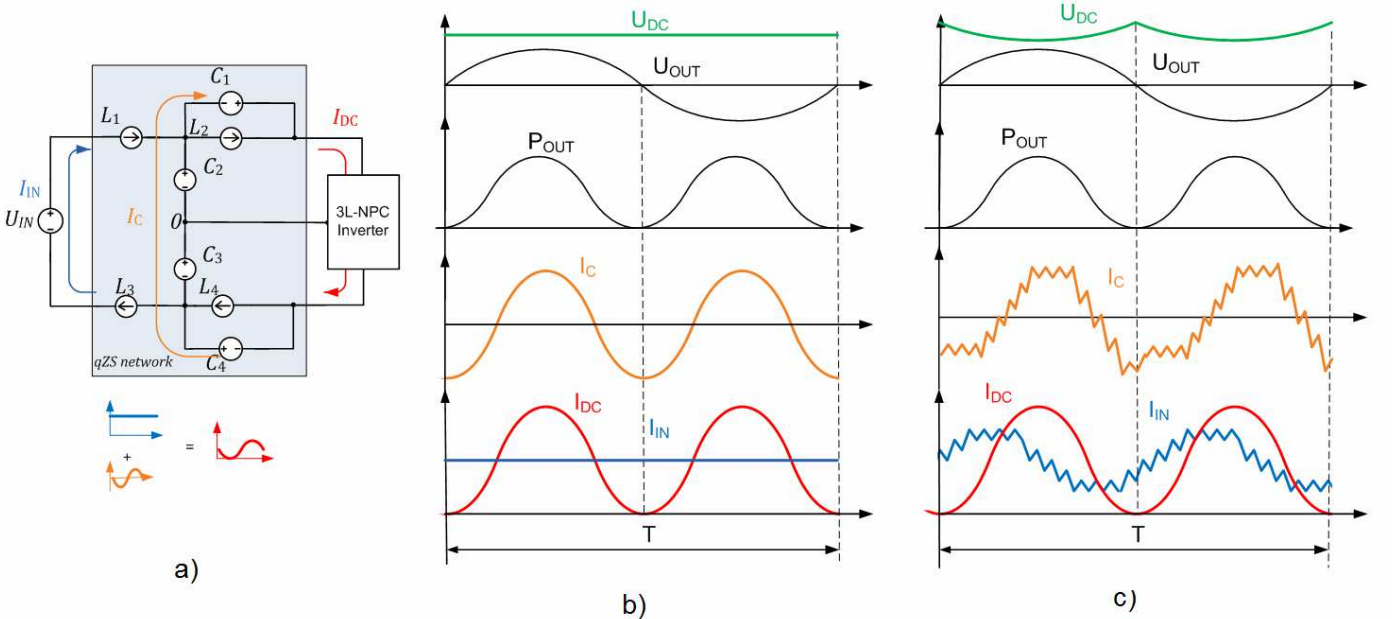


Fig. 4. Equivalent scheme and diagrams in the CCM.

Taking into account the CCM condition:

$$K_L = \frac{\Delta I_{L1}}{I_a} = \frac{U^2_{OUT_MAX} \cdot (1-2 \cdot D_S)}{2 \cdot (1-D_S) \cdot L \cdot P_{OUT}} T_S \cdot D_S, \quad (59)$$

and from Eqs. (49), (53) and (54) we can express:

$$L \geq \frac{U^2_{OUT_MAX} \cdot (1-2 \cdot D_S)}{2 \cdot (1-D_S) \cdot K_L \cdot P_{OUT}} T_S \cdot D_S. \quad (60)$$

It means that we can define the minimum value of the inductance in order to maintain the CCM operation of the proposed inverter.

IV. SIMULATION RESULTS

In order to verify theoretical background several simulations have been carried out. The first results cover the case with the output power of about 1 kW. Fig. 5 shows the obtained simulation results, listed from top to bottom: input current and input voltage (Fig. 5a), voltage across the capacitors (Fig. 5b), and output voltage before and after the filter (Fig. 5c). It is seen that inverter operates in the CCM and capacitor voltage ripple is about 10%. The capacitance value selected for $C_1 \dots C_4$ was 2.5 mF and inductance value set for $L_1 \dots L_4$ was 0.25 mH.

Next, the simulation was done for the light load and full power operating points. Fig. 6 shows the input current and capacitor voltage for 100 W and 5 kW (Figs. 6a and b, correspondingly). The main conclusion is that the CCM is unachievable with low output power.

It can be concluded that the capacitor value in a real system has to be larger than analytically predicted by (55) that is connected with power losses in the real system. Fig. 7 shows the dependences of the capacitor value that is necessary in order to obtain a voltage ripple lower than 10%. There are three cases presented: first is the theoretical prediction assuming ideal components and other two belong to the cases with winding resistances of the inductors of 0.01 Ω and 0.25 Ω , respectively. The main conclusion is that the capacitance value of the capacitors has to be increased with the losses due to the voltage drop in the DC-link and the requirement to keep the amplitude of the output voltage constant.

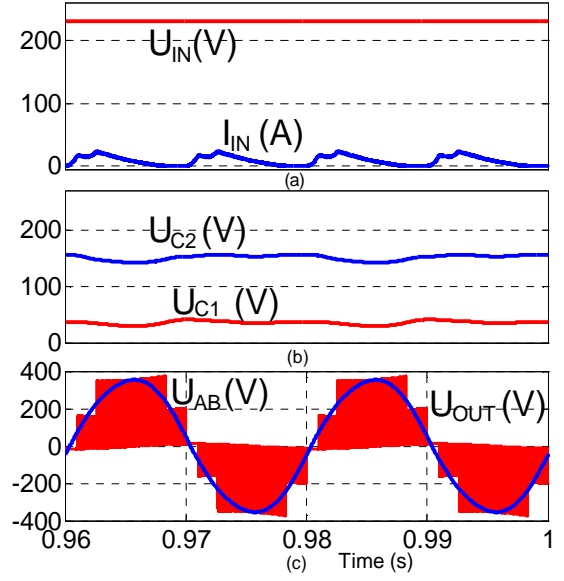


Fig. 5. Simulation results for 1 kW output power.

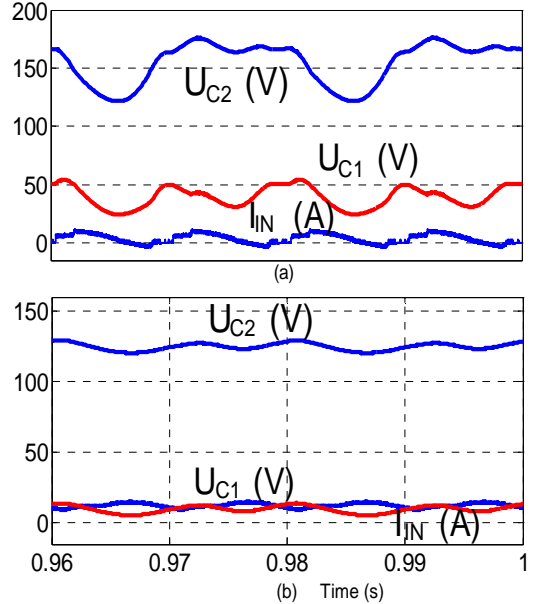


Fig. 6. Simulation results for 100 W (a) and 5 kW (b) output power.

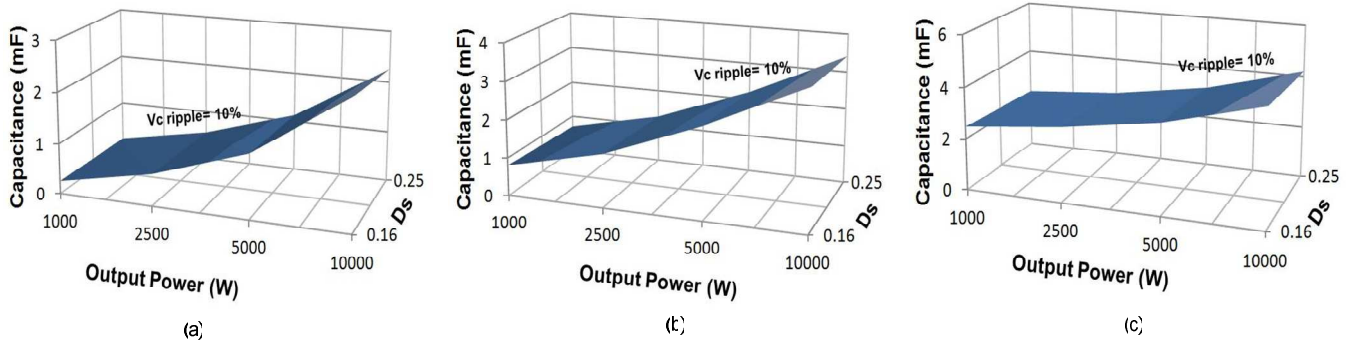


Fig. 7. Dependences of capacitance value C_1 on P_{OUT} and D_S .

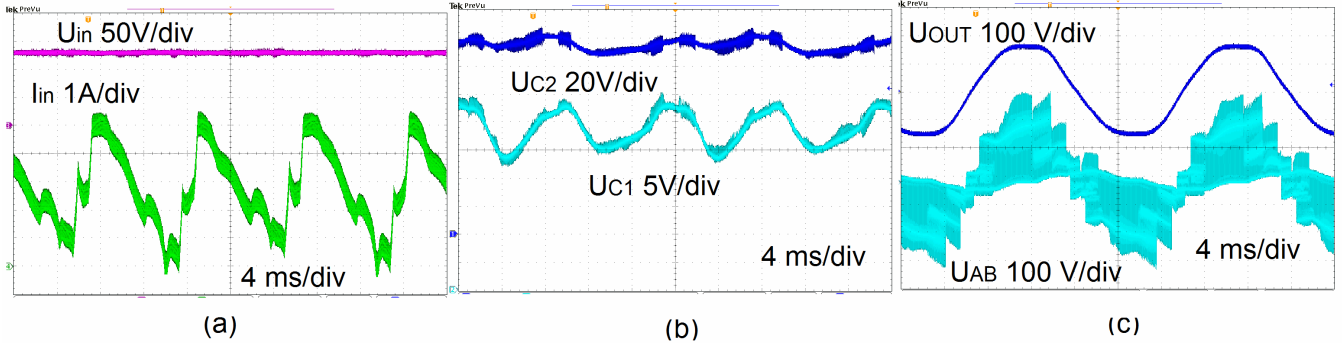


Fig.8. Experimental results for 200 W output power.

V. EXPERIMENTAL VERIFICATION

To verify the above presented assumptions a 500 W experimental setup was assembled. System parameters and component values used in the experiment are presented in Table I.

TABLE I. SYSTEM PARAMETERS AND COMPONENT VALUES USED FOR THE EXPERIMENT

Input DC voltage U_N	130 V
Output AC voltage U_{OUT}	110 V (RMS)
Capacitance value of the capacitors C_1, C_4	1160 μ F
Capacitance value of the capacitors C_2, C_3	920 μ F
Inductance value of the inductors $L_1 \dots L_4$	160 μ H
Inductance of the filter inductor L_0	4.4 mH
Capacitance of the filter capacitor C_0	240 μ F
Switching frequency	50 kHz

The control system is based on the FPGA board with EP2C5T144C8 from Altera. The ACPL-H312 drivers were chosen for a MOSFET transistor drive. Fig. 8 presents the experimental results. The input voltage was 130 V and output RMS voltage was 110 V. Carrier frequency was set to 50 kHz.

Fig. 8a shows the input current and voltage waveforms. It can be seen that the input current is on the border between the CCM and DCM. The voltages across the capacitors of the ZS network are shown in Fig 8b. As it can be seen, the capacitor voltages have a ripple of about 30%. The output voltage waveforms before and after the LC-filter are shown in Fig. 8c.

VI. CONCLUSIONS

The proposed single phase 3L-NPC qZSI is a combination of the quasi-Z-source inverter and the three-level NPC inverter. The 3L-NPC qZSI derives advantages from both topologies: it can buck and boost the input voltage; it has excellent short circuit immunity, due to the multilevel topology the higher power density is achievable.

In order to reduce the low frequency fluctuations of the DC-link voltage in a 3L-NPC qZSI large values of the capacitors are required. At the same time it is practically impossible to eliminate low frequency input current ripple completely, especially during the light load operating point. Such an effect will disappear in a symmetrically loaded three-phase system, because it is connected with the consumption of floating instantaneous power in a single-phase system. At the same time high frequency input current ripple is defined by the inductance value and switching frequency. Since the MOSFET transistors can be used in such topologies the switching frequency can be high

and as a result, the value of the inductance can be significantly decreased.

ACKNOWLEDGEMENT

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