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Single Phase Three-Level Quasi-Z-Source Inverter With a New Boost Modulation Technique

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***Abstract*— This paper describes a new modulation technique for a single phase three-level neutral-point-clamped qZS inverter. The proposed converter is intended for applications that require input voltage gain and high quality of the output voltage. The simulation and experimental results are presented and discussed.**

I. INTRODUCTION

A three-level neutral-point-clamped (3L-NPC) inverter has many advantages, such as lower semiconductor voltage stress, lower required blocking voltage capability, decreased *dv/dt*, better harmonic performance, soft switching possibilities without additional components, higher switching frequency due to lower switching losses, and balanced neutral-point voltage, in contrast to the two-level voltage source inverter. However, as a drawback, it has two additional clamping diodes per phase-leg and more controlled semiconductor switches per phase-leg than the two-level voltage source inverter. The 3L-NPC can normally perform only the voltage buck operation. In order to ensure voltage boost operation an additional DC/DC boost converter should be used in the input stage [1-2].

To obtain buck and boost performance the focus is on a quasi-Z-source inverter (qZSI). The qZSI was first introduced in [3]. The qZSI can buck and boost DC-link voltage in a single stage without additional switches.

The qZSI can boost the input voltage by introducing a special shoot-through switching state, which is the simultaneous conduction (cross conduction) of both switches of the same phase leg of the inverter. This switching state is forbidden for traditional voltage source inverters because it causes a short circuit of the DC-link capacitors. Thus, the qZSI has excellent immunity against the cross conduction of top and bottom-side inverter switches. The possibility of using shoot-through eliminates the need for dead-times without having the risk of damaging the inverter circuit. The input voltage is regulated only by adjusting the shoot-through duty cycle. In addition, the qZSI has a continuous mode input current (input current never drops to zero), which makes it especially suitable for renewable energy sources (e.g. fuel cells, solar energy, wind energy etc.). The main drawback of the qZSI is its poor performance in the case of small loads and relatively low switching frequency. In these conditions the qZSI starts to work in a discontinuous conduction mode, which causes an over-boost effect and leads to instabilities [3-7].

A three-level neutral-point-clamped quasi-Z-source inverter (3L-NPC qZSI,) proposed recently is a new modification of the qZSI. The new converter combines the advantages of the two topologies described above.

Fig. 1 illustrates the proposed topology of a 3L-NPC qZSI. Each leg of the 3L-NPC qZSI consists of two complementary switching pairs and four anti-parallel diodes. As an advantage, this topology can have continuous input current, the possibility to use shoot-through, lower switching losses and balanced neutral-point voltage in comparison with the traditional two-level voltage source inverter.

The inverter output voltage has three different levels: 0, $B\cdot(U_{IN}/2)$ and $B\cdot U_{IN}$ in the positive and negative directions, where B is the inverter boost factor. The shoot-through vector is generated separately during zero states. Finally, the shoot-though vector is mixed together with other control signals.

At the same time the shoot-through switching state demands new approaches in the modulation technique in order to combine the boost factor with the best possible voltage quality.

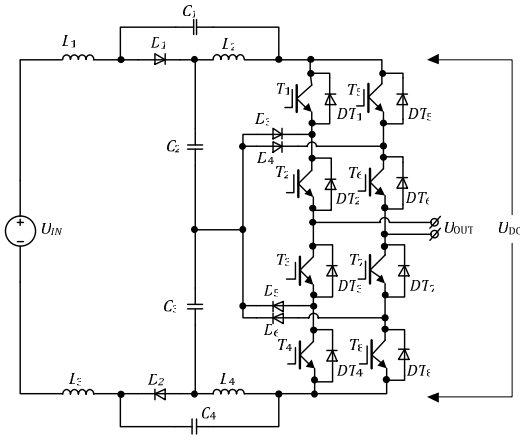

Fig. 1. Three-level neutral-point-clamped quasi-Z-source inverter (3L-NPC qZSI)

This paper is an attempt to improve the voltage quality of the 3L-NPC qZSI by a new modulation technique.

II. NEW MODULATION TECHNIQUE

There are several pulse width modulation (PWM) techniques that could be applied for the 3L-NPC qZSI [4], [11]-[14].The core idea of these methods is presented in Fig. 2. All of them generate the shoot-through states when the output voltage is in the zero state (U_{AB} = 0) in order to maintain constant and unaltered normalized average voltage per switching period whereas the shoot-through states are carefully and centrally added to the active states that enable the number of higher harmonics to be kept to a minimum.

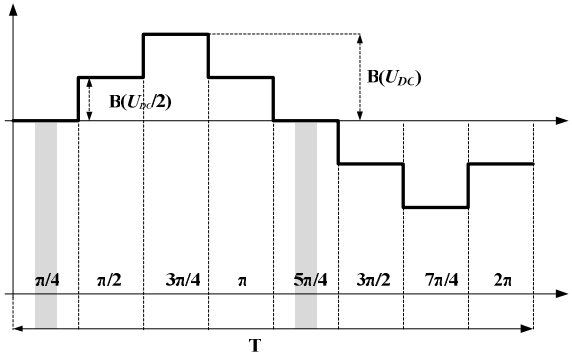

Fig. 2. Output voltage waveform of the traditional shoot-through PWM for the 3L-NPC qZSI.

Using these PWM techniques for the 3L-NPC qZSI, the U_{AB} has only two zero states per period and shoot-through states can only be placed during these two intervals ([0, π/4] and [π, 5π/4]).

These techniques present some problems, such as a larger size of the passive elements, more input current ripple and capacitor voltage disbalance.

A. Description of General Principles

Fig. 3*a* shows a sketch of the proposed modulation technique.

One modulating sinusoidal wave and four triangular carriers are compared to obtain the different states of T_1, T_2, T_5 and T_6 and T_3, T_4, T_7 and T_8 have the complementary state of the other, respectively.

Carrier$_1$ is used to generate the shoot-through states in comparison with a constant value that includes the desired D_s value. Operating in this way, uniformly distributed shoot-through states with the constant width during the whole output voltage period can be achieved.

In order to compensate the average voltage U_{AB} when the shoot-through states are applied, leg *B* must compensate this situation through the change of the voltage U_{B0}. Fig. 3*b* shows how we can obtain this compensation.

During the positive semi-cycle, leg *B* has to produce $U_{B0} = -U_{dc}/2$ more times to restore the average voltage U_{AB}. This is produced through *carrier*$_4$ displacement that generates the pulses of T_6. During the negative semi-cycle the same situation is produced. Leg *B* has to produce $U_{B0} = +U_{dc}/2$ more times to restore the average voltage U_{AB}. This is produced through *carrier*$_3$ displacement that controls the pulses of T_5.

The resulting waveform of the output voltage before the output filter is shown schematically in Fig. 3*c*.

B. Boost Regulation Capability

In the proposed modulation technique the desired boost is reached because the shoot-through states are distributed with a constant width during the whole output voltage period and the qZ stage is working at the maximum frequency. Furthermore, by this technique we can use the ratio between the modulation index (*M*) and the maximum shoot-through duty cycle D_{S_MAX} (1) and the ratio between *B* and D_s (2):

$$D_{S\_MAX} \le 1 - M\ , \tag{1}$$

$$B = \frac{U_{DC}}{U_{IN}} = \frac{1}{1 - 2 \cdot D_S}. \tag{2}$$

As a result, taking into account (1) the maximum value of the output voltage we obtain

$$U_{MAX\_OUT} = U_{IN} \cdot M \frac{1}{(1 - 2 \cdot D_S)}. \tag{3}$$

Using the maximum possible value of the modulation index, the amplitude of the output voltage can be estimated as

$$U_{MAX\_OUT} = U_{IN} \cdot \frac{1 - D_S}{(1 - 2 \cdot D_S)}. \tag{4}$$

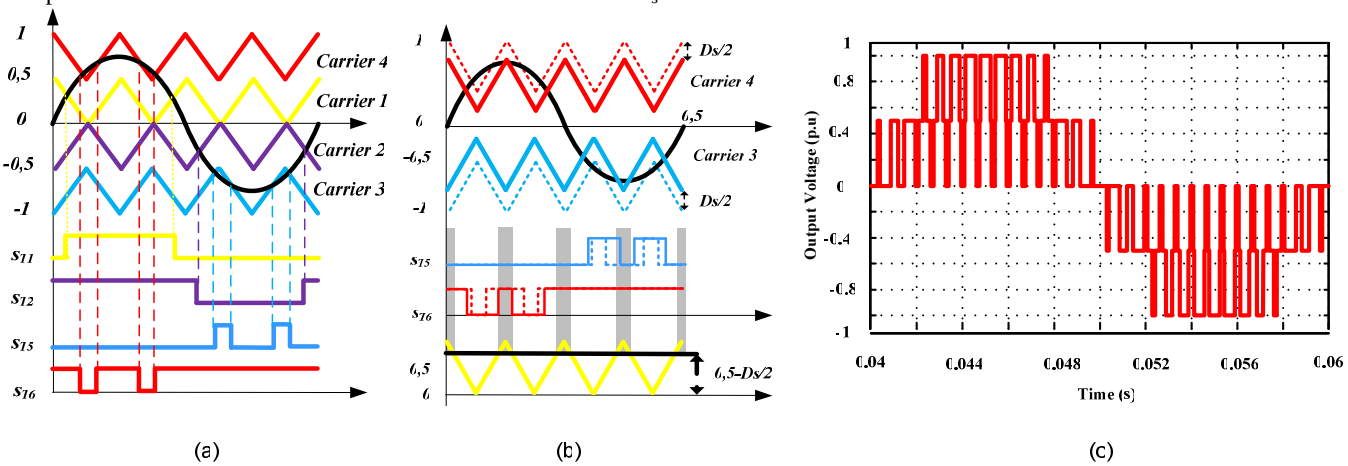

Fig. 3. Sketch of the proposed modulation technique with uniformly distributed shoot-through states and constant width.

III. Simulation and Experimental Verification of The Proposed Modulation Technique

To verify the proposed modulation technique a small power scaled experimental board was assembled. Preliminary verification was done by help of a simulation model assembled in the SimPowerSystems of Matlab/Simulink.

A. System Parameters

The values of the parameters of the qZS network and the output filter are presented in Table I.

TABLE I. System Parameters Used for Simulations and Experiments

Control Unit (FPGA)	Cyclone II EP2C5T144C8
Driver Chip	ACPL-H312
Input DC voltage U_N	30 V
Output AC voltage U_{OUT}	30-40 V
Capacitance value of the capacitors C_1 ... C_4	240 uF
Inductance value of the inductors L_1 ... L_4	230 uH
Inductance of the filter inductor L_0	4.4 mH
Capacitance of the filter capacitor C_0	240 uF
Switching frequency	25 kHz

The control system is based on the FPGA board with EP2C5T144C8 from Altera. The ACPL-H312 drivers were chosen for a MOSFET transistor drive.

B. Simulation Results

Our first simulation results were obtained from a case without a shoot-through station. Fig. 4 presents the results of the simulation. The simulation waveforms correspond to the operating point with 27 V input DC voltage and 26 V output AC voltage. Carrier frequency was set up to 25 kHz.

Fig. *4a* shows the input current and voltage waveforms. It can be seen that the input current has a discontinuous behavior.

The voltages across the capacitors of the ZS network are shown in Fig 4*c*. The DC-link is shown in Fig 4*b*. As it can be seen, capacitor voltages are not stable enough in order to provide a constant level of the DC-link voltage.

Voltage and current across transistor T1 are shown in Fig. 4*d*. At the same time the voltage and current across transistor T5 are shown in Fig. 4*e*. It is shown that despite the fact that transistors are on top of the different legs they are not equally loaded. This relates the modulation technique. According to the proposed algorithm, leg A is in response for output voltage sign and leg B is in response for sinusoidal waveform of output voltage. The output voltage waveforms before and after the LC-filter are shown in Fig. 4*f*. The THD of the output voltage is about 9.5%. It is evident that in this case the quality of the output voltage is not sufficient. It is because of the disbalance of the DC-link voltage caused by the uneven distribution of power consumption in the load. The moment of time with the maximum value of the output voltage corresponds to the maximum power consumption. As a result, the input current and capacitor voltage have significant fluctuations.

One of the ways to improve the quality of the output voltage is to increase passive element values. It is a regressive way. The other approach is to embed a shoot-through station that is equally distributed during the full duty cycle. This modulation technique was developed specially for our study purposes.

Our second simulation results were obtained from a case with a shoot-through station. Fig. 5 represents the similar results of the simulation that correspond to the operating point with 27 V input voltage and 33 V output AC voltage. The shoot-through duty cycle D_s=0.16 has the same carrier frequency. It is evident that the input current is closer to a continuous mode. It should be noted that the amplitude of the current has slightly decreased. As it can be seen, capacitor voltages are more stable as compared to the previous case. As a result, the THD of the output voltage has improved up to 8%.

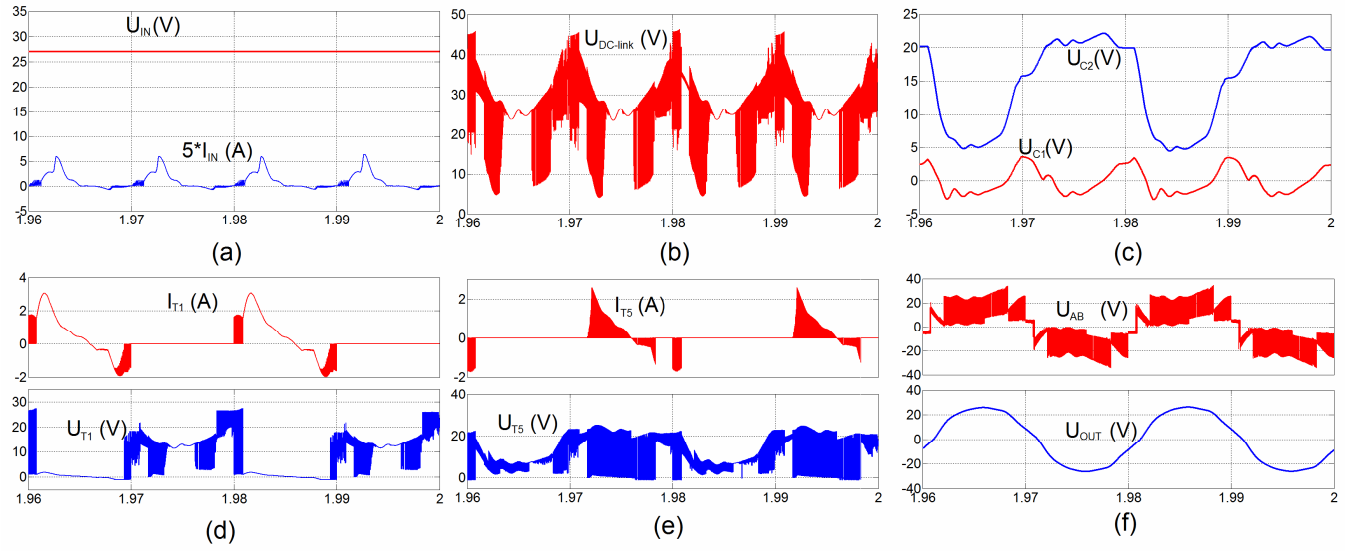

Fig. 4. Simulation results of NPC qZSI without shoot-through states.

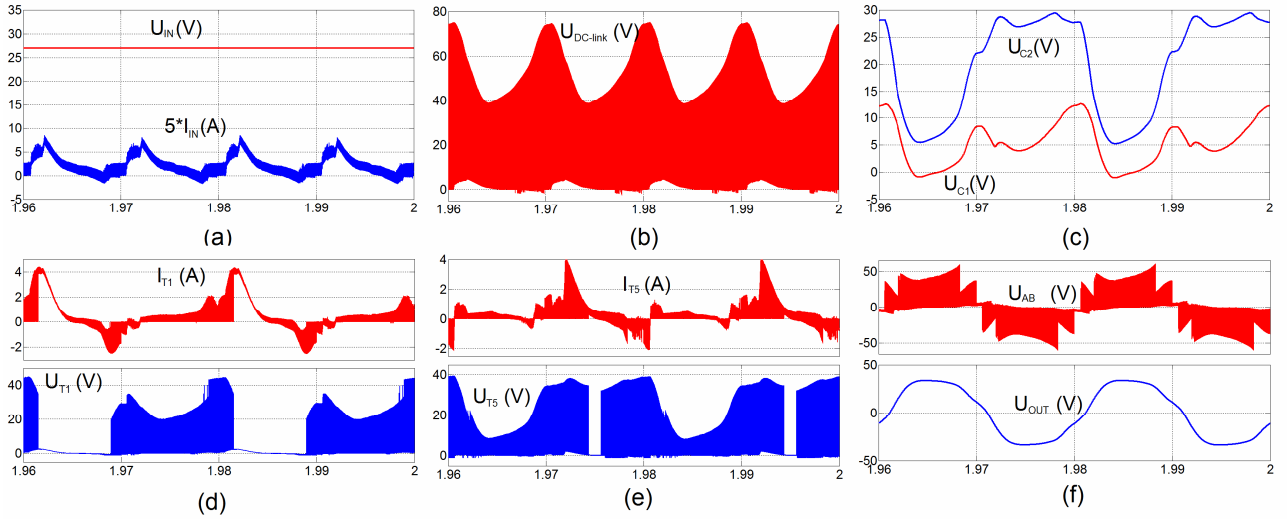

Fig. 5. Simulation results of NPC qZSI with the shoot-through duty cycle D_s=0.16.

In the further investigation , focus was on the simulation study of dependences between the shoot-through duty cycle versus the output voltage quality (THD) and the boost capability (B), shown in Fig. 6.

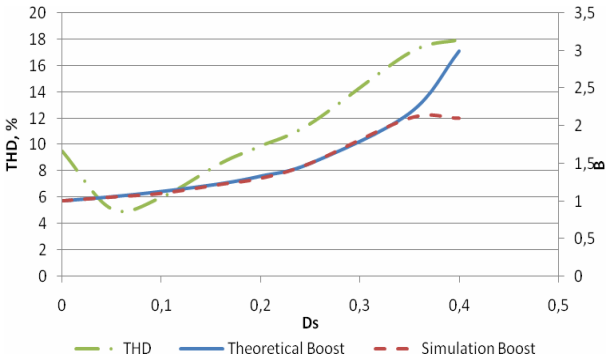

Fig. 6. Simulation results of the shoot-through duty cycle D_s versus THD and the boost capability B.

From Fig. 6 it is evident that there are some optimal operation points with the highest output voltage quality and the maximum boost factor. The highest output voltage quality was achieved with D_S equal to 0.05 and the maximum boost factor was obtained with D_S equal to 0.35. Also, from Fig. 6 it is evident that the behavior of the boost factor is similar to the theoretically estimated value Eq. (4), especially in the domain with a low shoot-through duty cycle value. Differences in the quantities are connected to the losses in the components and the discontinuous current mode that is a common tendency with the qZS family converters.

C. *Experimental Results*

To verify the proposed modulation technique and the results of the simulation a small power laboratory prototype was assembled.

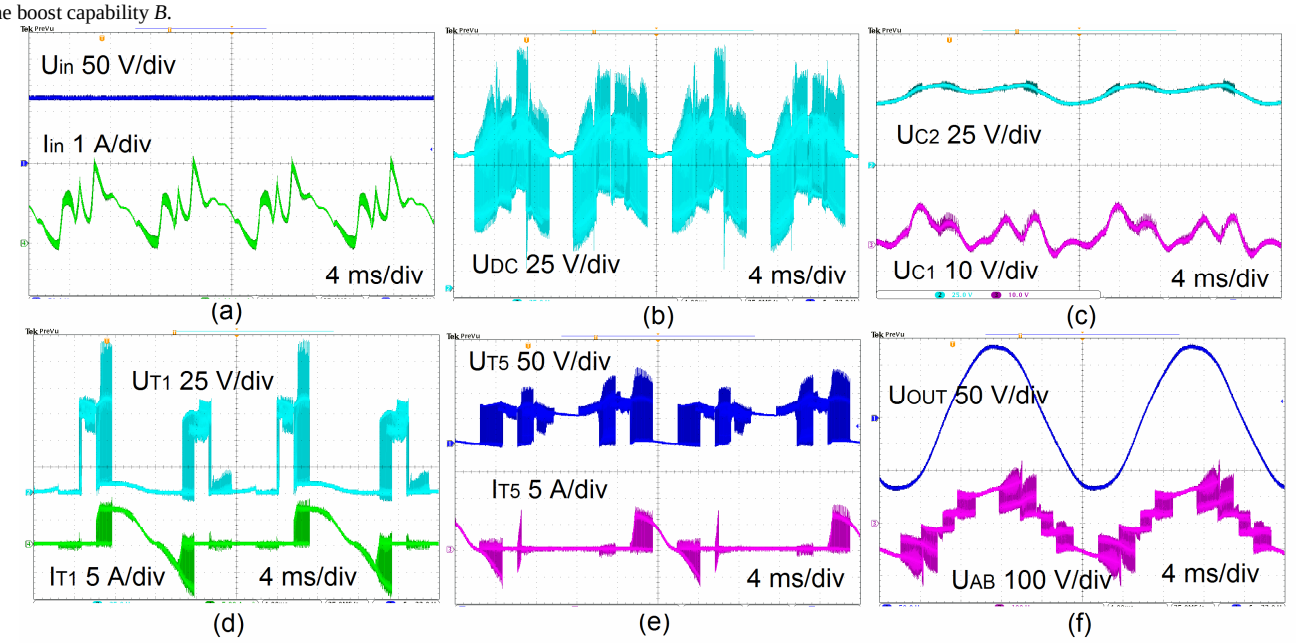

Fig. 7. Experimental results of the NPC qZSI without shoot-through states.

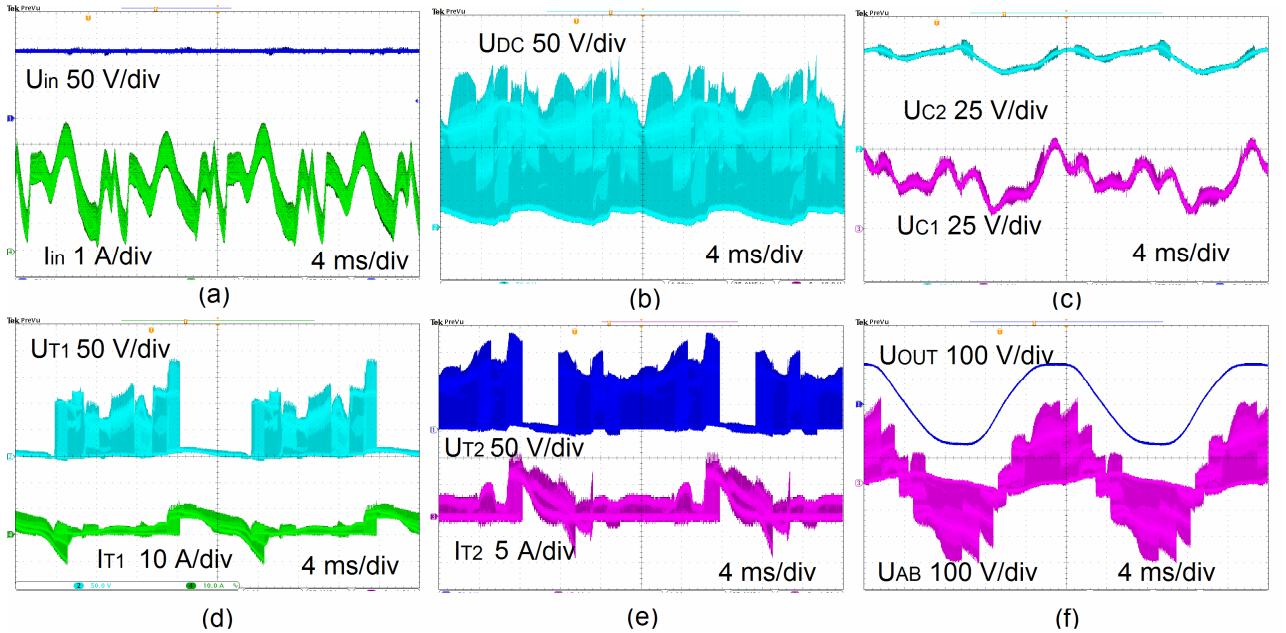

Fig. 8. Experimental results of the NPC qZSI with the shoot-through duty cycle D_s=0.16.

Experimental investigations were carried out according to the simulation. Fig. 7 presents the results of the experiment without a shoot-through station. The input current and voltage waveforms are shown in Fig. 7*a*. It is seen that the input current has significant ripple and a discontinuous behavior.

The voltages across the capacitors *C1* and *C2* of the ZS network are shown in Fig 7*c*. The capacitors *C3* and *C4* have similar voltage diagrams. The DC-link is shown in Fig 7*b*. As it can be seen, capacitor voltages are not stable enough to provide a constant level of the DC-link voltage. The voltage on the capacitor *C1* is dropping up to below zero.

Voltage and current across transistor T1 are shown in Fig. 7*d*. At the same time, the voltage and current across transistor T5 are shown in Fig. 7*e*. It is proved that despite the fact that transistors are on top of the different legs they are not equally loaded.

The output voltage waveforms before and after the LC-filter are shown in Fig. 7*f*. The THD of the output voltage is about 14%. It is evident that in this case the quality of the output voltage is not good enough.

In general, experimental results proved the expected converter behavior. The main difference lies in the slight asymmetrical waveform of the output voltage. It is connected with the asymmetrical switching of the transistors. It evokes asymmetrical charging of the boost capacitors of the drivers that were used in the experimental board.

Fig. 8 represents similar results with the shoot-through duty cycle D_s=0.16.

Fig. 8*a* shows the input current and voltage waveforms. It is evident that the input current is on the boundary between the CCM and DCM. Voltage and current across transistors T1 and T5 are shown in Figs. 8*d* and 8*e*, respectively. The voltages across the capacitors of the ZS network are shown in Fig 8*c*. As can be seen, capacitor voltages are more stable than in the previous case. As a result, the THD of the output voltage is improved up to 7.6%. The output voltage waveforms before and after the LC-filter are shown in Fig. 8*f*.

The shoot-through duty cycle equalized the asymmetrical switching of the transistors that provided charging for the boost capacitors of the drivers. As a result, the behavior of the converter becomes stable and predictable. In this case, our experimental results are in good agreement with the simulation. In conclusion, it should be noted that the chosen transistor drivers that were not used before in such topologies are a good solution when the shoot-through duty cycle is present.

The diagrams presented above show that the main problem lies still in the DCM that evokes fluctuations of the input current. It is also evident that as a result of the DCM of the input current, the oscillating processes that happen in the qZS network do not evoke a constant behavior of the DC-link voltage. The DC-link voltage is significantly dropping during maximum output power consumption and rising during minimum output voltage. It has a significant influence on the quality of the output voltage that can be improved by increasing the capacitor value.

Further experimental investigation of the proposed modulation technique was carried out according to Fig. 6. Dependences between the shoot-through duty cycle versus the quality of the output voltage (THD) and the boost capability (B) are shown in Fig. 9.

It is evident that shoot-through improves the quality of the output voltage. At the same time, with a further increase of the shoot-through duty cycle boost factor *B*, a simultaneous increase occurs with THD. It is additionally illustrated in Fig. 10 where output voltages before and after the LC-filter for different D_S are shown. The best output voltage waveform is achieved with the lowest D_S. Its increase leads to the increase of the DC- link fluctuations that spoil the output voltage waveform. At the same time, it is not a drawback of the

proposed modulation technique because it depends on the values of the passive components of the qZS network.

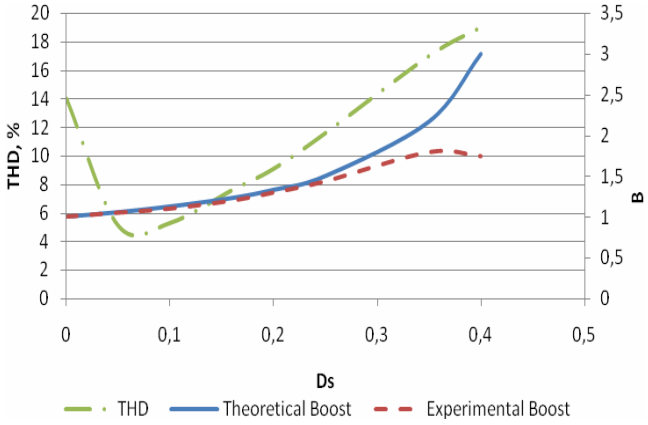

Fig. 9. Experimental results of the shoot-through duty cycle D_s versus THD and the boost capability B.

IV. CONCLUSIONS

This paper describes an NPC qZSI with a new modulation technique of the distributed shoot-through duty cycle. The theoretical and experimental results prove that the proposed modulation technique is relevant because of its ability to combine the necessary boost factor with the good quality of the output voltage.

As a result, the topology of the discussed DC/AC converter becomes more suitable for photovoltaic or fuel cell applications where controlled boost capability with a good output voltage quality are required.

Distributed shoot-through duty cycle allows balancing of the DC-link voltage and a decreasing value of passive components.

Further improvements require that the discontinuous input current mode be eliminated and DC-link voltage stabilized. A solution could be to develop a closed loop control system with an additional shoot-through duty cycle regulation capability. At the same time this problem will disappear in a three- phase system with a symmetrical load where instantaneous power consumption is constant.

Thus, the proposed modulation technique can be especially beneficial in a three-phase system.

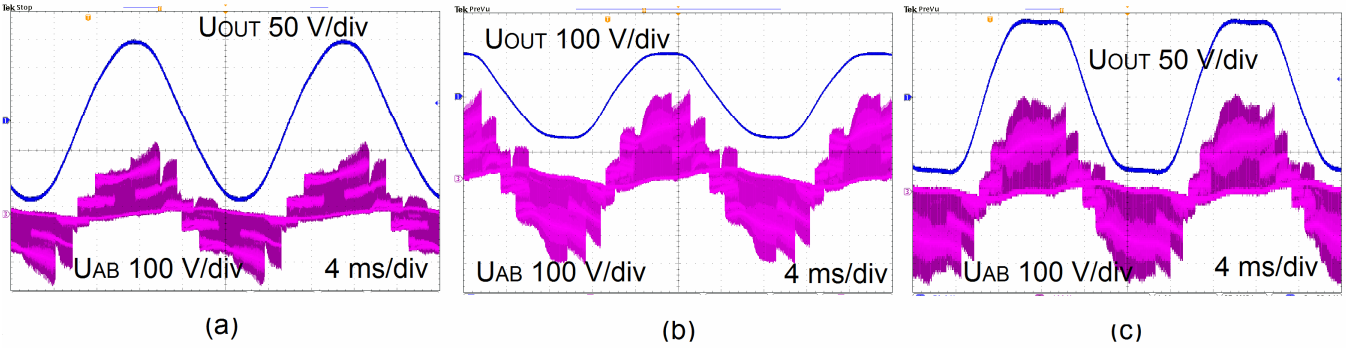

Fig. 10. Experimental output voltage waveforms with different D_S: a) D_S=0.04; b) D_S=0.10; c) D_S=0.25.

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