High-Efficiency Single-Phase PFC Rectifier Analysis

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Abstract. *The article is devoted to analysis of the power factor correction (PFC) rectifier performance. The use of a zero-current switching quasi-resonant pulse converter instead of a conventional boost converter at the power stage of PFC rectifier is proposed and analyzed. A steady-state current error as a stabilization accuracy criterion has been analyzed for different structures of two-loop closed control system. The input current quality for different control methods has been assessed by means of total harmonic distortion (THD) and true power factor (PF$_{true}$).*

Keywords

Energy efficiency, high-frequency converters, power factor correction (PFC), single-phase rectifiers, total harmonic distortion (THD).

1. Introduction

Nowadays the problems devoted to electrical energy quality and energy efficiency are of great importance [1]. These issues appear particularly due to the fast development of Smart Grid concept and since the number of renewable energy sources is continuously growing [2]. Voltage and current harmonics produced by nonlinear loads increase power losses and therefore have a negative impact on electric utility distribution system and components. Higher harmonics increase power losses in transformers and transmission lines and can shorten their lifetime. Therefore, satisfaction the power quality requirements (total harmonic distortion limits for current and voltage) is extremely urgent issue [3].

A number of works devoted to this topic show description, analysis and comparison of different power factor correction (PFC) converters [4] which are used for improvement the energy efficiency in various applications e.g. uninterruptible power supplies (UPS). Special attention is paid to the performance of PFC and possibility to build them utilizing unified power modules.

The main parameters of the PFC performance are efficiency and power factor, which depend on the switching frequency. An integrated approach to the implementation of PFC takes into account the power factor, harmonic distortion and the efficiency of the converter [5].

The known PFC circuits are usually performed on the basis of conventional parallel pulse converters [6], [7]. In their current loops non-optimal regulators are often used based on so-called reverse-current amplifiers. To improve efficiency of PFC at high frequency in [8] multiphase pulse converters are used. They are critical in terms of extra expenses as well as from the point of view of ensuring an adequate stability reserve of the closed-loop system. There is quite limited amount of works devoted to the problems of PFC subharmonic stability [9], [10]. In some articles these issues have not got enough attention [11].

The family of quasi-resonant pulse converters (QRPC) was described in details in [12]. Implementation of QRPC with zero current switching (ZCS) into PFC allows to reduce power losses maintaining high efficiency at high switching frequency and obviously improve power factor. However, high switching frequency raises the problem of improving the speed of the current loop in PFC. The main task of the current loop is to ensure a minimal deviation of the input current regarding to reference sine wave in real time. The problem of high-speed PFC current loop synthesis has been investigated in [13].

An approach based on continuous approximate models for investigation AC/DC converters with active PFC is presented in [14]. The processes in single-loop PFC with conventional parallel pulse converter with zero-current turning on switch are investigated using method of averaging in [15]. In other words, transistor works in boundary conduction mode (BCM), i.e. it is on the border between continuous conduction mode (CCM) and discontinuous conduction mode (DCM). In our view, such decision yields the way of using QRPC-ZCS, in which high-frequency current ripple and turn off power losses are minimal. In this case, the negative impact of the QRPC-ZCS variable switching frequency on the filtering quality of input current harmonics can be reduced to minimum due to its increase up to several MHz.

The problems of PFC closed-loop control system implementation were discussed in [16], [17] as well as estimation the input current quality for different PFC topologies and control methods [18]. The aim of this work is comprehensive description of the main features of the PFC development and analysis of their work, including power quality and stabilization issues, as well as the formation of completed findings.

2.   PFC Rectifiers Description

First of all, we will consider the simplified schemes of PFC based on classical boost converter and the one based on QRPC-ZCS. Fig. 1 represents the rectifier with active PFC circuit based on conventional boost converter. The input of the circuit is connected to supply AC voltage network. The output DC voltage value is $V_{out} = 360V$. The load resistance is $R = 120\Omega$. Thus, the output power of the converter is $P_{out} = 1080W$.
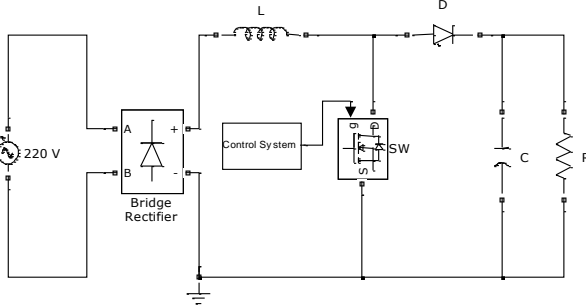

Fig. 1.   A simplified scheme of rectifier with conventional PFC.

Fig. 2 illustrates the rectifier with active PFC circuit based on zero-current-switching quasi-resonant pulse converter. The main parameters are the same as of conventional PFC, except the presence of the parallel resonant circuit L_rC_r. It provides zero current switching of the power switch SW and thus significantly reduces the switching losses and improves efficiency.
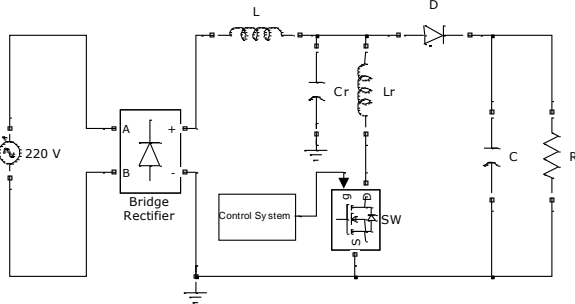

Fig. 2.   A simplified scheme of rectifier with PFC based on zero-current switching quasi-resonant pulse converter.

Since frequency modulation is used to control the QRPC-ZCS, the duty cycle of the control signal must satisfy the condition of the switching at zero current:

$$T_0 = 2\pi\sqrt{L_rC_r} \qquad (1)$$

where T_0 is the switching period of the resonant circuit L_rC_r, the resonant inductance $L_r = 6.1\mu H$, the resonant capacitance $C_r = 220nF$. The operation of quasi-resonant converters is described in details in [12].

The values of the passive elements of both circuits were calculated according to [16] and they are as follows: the input storage inductance $L = 820\mu H$, the output filtering capacitance $C = 300\mu F$. The selection was made assuming the input current ripple in the storage inductor is 20% and the ripple of output voltage is 5%.

3.   Control System Analysis

The block diagram in Fig. 3 shows the detailed structure of the PFC based on QRPC-ZCS and its control system. The circuit contains the storage inductor L, the resonant circuit L_rC_r, the power switch SW, the isolating diode D, the filtering capacitor C and the load resistor R. The PFC control system comprises current loop controller (CL) and voltage loop controller (VL), current sensor (CS) and voltage sensor (VS), squarer (SQ), divider (DV), multiplier (M), switch control unit (Ctrl), reference current generation unit (U_R/R_0), where U_R is rectified voltage and R_0 is resistor specifying the reference current.
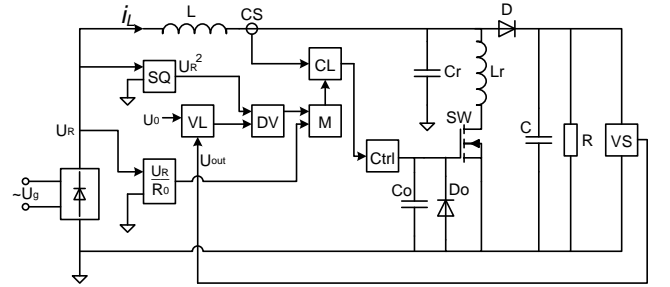

Fig. 3.   The detailed structure of PFC with two-loop control system.

The dynamic models for control system investigation were presented in [13] and detailed analysis of steady-state current error for different structures of two-loop control system of PFC was provided in [18]. The results of calculation are shown in Fig. 4. The presented curves show the accuracy of current stabilization for control system with main voltage loop including squarer, divider and multiplier (curve 1), with main current loop including multiplier (curve 2), with main current loop including squarer, divider and multiplier (curve 3), with main current loop without squarer, divider and multiplier (curve 4).
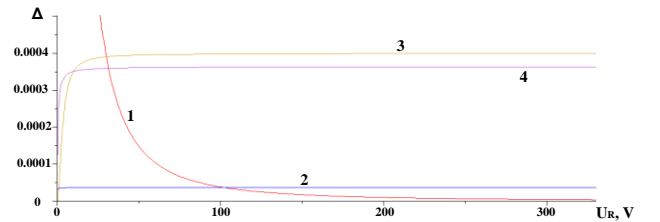

Fig. 4.   Steady-state current error for various structures of PFC control systems.

As could be seen (Fig. 5), the control structure with main voltage loop in the presence of the squarer, divider, multiplier (commercially available IC UC3854) has the smallest averaged current error as well as the proposed structure with main current loop without squarer and divider (curves 1 and 2, respectively). However, at low input voltage the current error in the structure with main current loop (curve 2) is considerably less than in the structure with main voltage loop (curve 1).

At the maximum input voltage current error in the structure with main voltage loop is more than 2 times lower than in the one with main current loop. However, it should

be noted that the actual current error in the real system with main voltage loop is much higher than the analytically calculated values (curve 1) throughout the range of U_R. The reason for this phenomenon is that the input current loop obtains the product of reference current and voltage stabilization error, comprising the fundamental frequency component of the rectified voltage. The impact of this feature on the input current distortion is studied in [11].

4. Input Current THD and Power Factor Analysis

For non-sinusoidal situations voltages and currents contain harmonics. Some harmonics are caused by system nonlinearities such as transformer saturation, most harmonics are produced by power electronic loads such as adjustable-speed drives and diode-bridge rectifiers, as we have. When steady-state harmonics are present, voltages and currents may be represented by Fourier series

$$v(t) = \sum_{k=1}^{\infty} V_k \sin(k\omega_0 t + \delta_k), \quad i(t) = \sum_{k=1}^{\infty} I_k \sin(k\omega_0 t + \delta_k) \quad (2)$$

and their root mean square values will be

$$V_{rms} = \sqrt{\sum_{k=1}^{\infty} \frac{V_k^2}{2}} = \sqrt{\sum_{k=1}^{\infty} V_{krms}^2}, \quad I_{rms} = \sqrt{\sum_{k=1}^{\infty} \frac{I_k^2}{2}} = \sqrt{\sum_{k=1}^{\infty} I_{krms}^2} \ . (3)$$

The average power is given by

$$P_{avg} = \sum_{k=1}^{\infty} V_{krms} I_{krms} \cos(\delta_k - \theta_k) = P_{1avg} + P_{2avg} + P_{3avg} + \ldots \quad (4)$$

where we can see that each harmonic makes a contribution to the average power.

A frequently-used measure of harmonic levels is total harmonic distortion (THD) of distortion factor, which is the ratio of the root mean square value of the harmonics (above fundamental) to the root mean square value of the fundamental times 100% [19] or

$$THD_V = \frac{\sqrt{\sum_{k=2}^{\infty} V_{krms}^2}}{V_{1rms}} \cdot 100\% = \frac{\sqrt{\sum_{k=2}^{\infty} V_k^2}}{V_1} \cdot 100\% \ , \quad (5)$$

$$THD_I = \frac{\sqrt{\sum_{k=2}^{\infty} I_{krms}^2}}{I_{1rms}} \cdot 100\% = \frac{\sqrt{\sum_{k=2}^{\infty} I_k^2}}{I_1} \cdot 100\% \ . \quad (6)$$

If we substitute (5) and (6) into (3), we find that

$$V_{rms} = V_{1rms} \sqrt{1 + \left(\frac{THD_V}{100}\right)^2}, \quad I_{rms} = I_{1rms} \sqrt{1 + \left(\frac{THD_I}{100}\right)^2} \ . \quad (7)$$

The concept of power factor originated from the need to quantify how efficiently a load utilizes the current that it draws from an AC power system. The true power factor is the ratio of average power P_{avg} to apparent power S:

$$PF_{true} = \frac{P_{avg}}{S} = \frac{P_{avg}}{V_{rms} I_{rms}} \ . \quad (8)$$

Thus substituting (7) into (8) yields the following exact form of true power factor:

$$PF_{true} = \frac{P_{avg}}{V_{1rms} I_{1rms}} \cdot \frac{1}{\sqrt{1 + \left(\frac{THD_V}{100}\right)^2} \cdot \sqrt{1 + \left(\frac{THD_I}{100}\right)^2}} \ . \quad (9)$$

Taking into account assumptions that in most cases the contributions of harmonics to average power are small ($P_{avg} \approx P_{1avg}$) and since THD_V is usually less than 10%, then $V_{rms} \approx V_{1rms}$. Incorporating these two assumptions into (9) yields approximately form for true power factor:

$$PF_{true} = \frac{P_{1avg}}{V_{1rms} I_{1rms}} \cdot \frac{1}{\sqrt{1 + \left(\frac{THD_I}{100}\right)^2}} = PF_{disp} \cdot PF_{dist} \ . \quad (10)$$

Since the displacement power factor PF_{disp} can never be greater than unity, the true power factor PF_{true} has the upper bound limited by the distortion power factor PF_{dist}

$$PF_{true} \leq PF_{dist} = \frac{1}{\sqrt{1 + \left(\frac{THD_I}{100}\right)^2}} \ . \quad (11)$$

The waveforms of the PFC operation with one current loop control system were obtained based on simulation performed in Matlab Simulink. The detailed description of control system is given in [16]. The results of simulation are shown in Fig. 5.
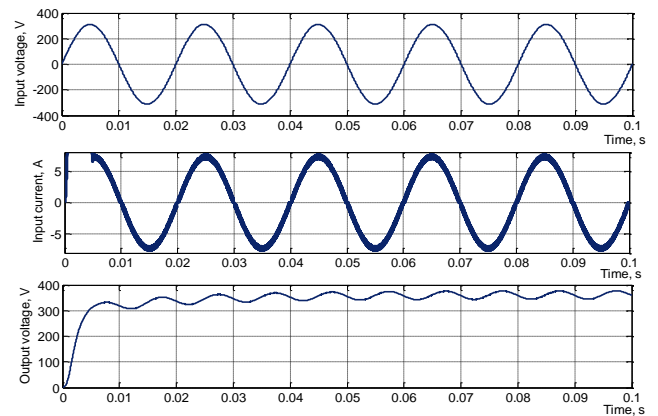

Fig. 5. Simulation results of PFC operation: input voltage, input current, output voltage.

The grid voltage has not significant distortions and THD_V is near 1%. Thus the assumptions made for assess the power factor by (10) are valid.

As could be seen in steady-state the output DC voltage is near 360V with low-frequency ripple up to 5%. This confirms the correctness of the choice of the output capacitor value and demonstrates that voltage feedback for two-loop control system will comprise the fundamental frequency component of the rectified voltage.

The input current is close to sinusoidal form and has relatively low level of THD_I. Thus the main task of power factor correction is performed. An input current spectrum for PFC based on conventional boost converter with standard pulse-width modulation (PWM) control at 100 kHz switching frequency is shown in Fig. 6. The level of current distortion is characterized by $THD_I = 10.34\%$. The true power factor in this case is $PF_{true} = 0.9947$.
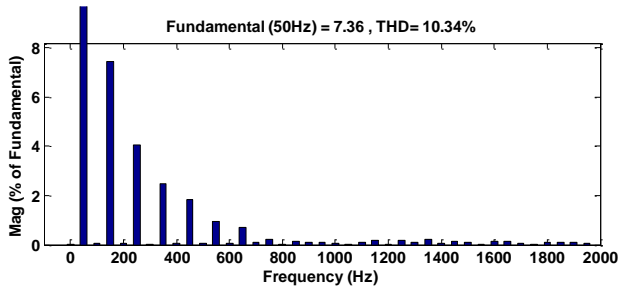

Fig. 6. The input current THD analysis for PFC based on conventional boost converter with PWM control.

An input current spectrum for PFC based on conventional boost converter with hysteresis control is shown in Fig. 7. Both frequency and duty cycle were variable within the one period of rectified voltage. The level of input current distortion is $THD_I = 3.12\%$. The true power factor in this case is $PF_{true} = 0.9995$.
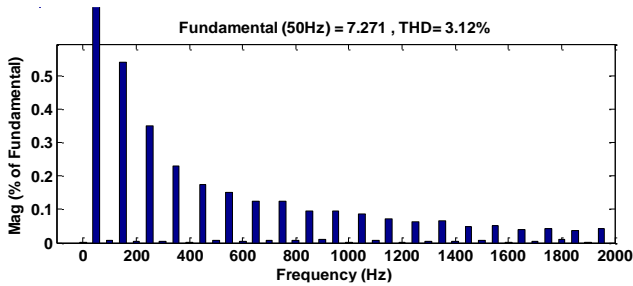

Fig. 7. The input current THD analysis for PFC based on conventional boost converter with hysteresis control.

An input current spectrum for PFC based on zero-current switching quasi-resonant pulse converter with frequency modulation (FM) control is shown in Fig. 8. The duty cycle of control signal was adjusted according to (1) while the switching frequency was changing above 100 kHz. The level of input current distortion is characterized by $THD_I = 8.85\%$. The true power factor in this case is $PF_{true} = 0.9961$.
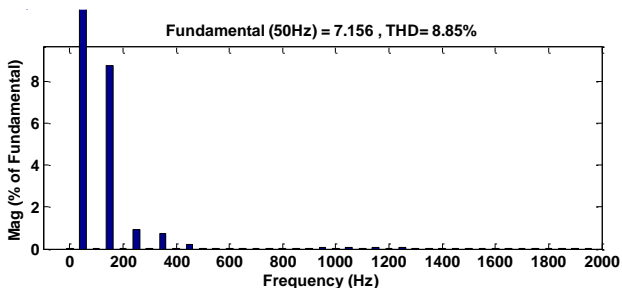

Fig. 8. The input current THD analysis for PFC based on quasi-resonant pulse converter with FM control.

5.   Conclusions

The main components of PFC rectifier energy efficiency have been analyzed in this study. The use of ZCS-QRPC as power stage of PFC allows reducing power losses maintaining high efficiency at high switching frequency. The nominal switching frequency as usual used for these converters varies from hundreds kHz to few MHz. Thus, their advantages are not so evident at 100 kHz switching frequency, which is typical for PWM converters.

A steady-state current error as a stabilization accuracy indicator has been analyzed for different structures of the control system of PFC. The structure with main voltage loop in the presence of the squarer, divider, and multiplier has the smallest averaged current error as well as the proposed structure with main current loop without squarer and divider ($\sim10^{-5}$). However, at low input voltage the current error in structure with main current loop is considerably less than in structure with main voltage loop.

The input current and true power factor of PFC have been analyzed. The input current quality of PFC based on ZCS-QRPC ($THD_I = 8.85\%$) is better than in PFC based on conventional boost converter with PWM ($THD_I = 10.34\%$), but worse than in one with hysteresis control ($THD_I = 3.12\%$). At the same time, a true power factor for all structures is above 0.99. The input current spectra meet the requirements of IEC 61000-3-2 for class A equipment.

Acknowledgements

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